amplifying transistor is connected to a drain terminal of the p-channel biasing transistor, and a source terminal of the p-channel biasing transistor is connected to a biasing side power source line comprising:

increasing an electric potential of an output terminal through the p-channel biasing transistor during a first period, wherein the output terminal is connected to a source terminal of the p-channel amplifying transistor;

decreasing the electric potential of an output terminal through the p-channel amplifying transistor during a second period;

wherein a gate potential of the p-channel biasing transistor during the first period is lower than a gate potential of the p-channel biasing transistor during the second period.

REMARKS

It is believed that no new matter is being added. Applicant is submitting herewith a check of $408 for the new claims (for claims in excess of 20 = 4x$18) (for independent claims in excess of 3 = 4x$84). If any further fee should be due, please charge our deposit account 50/1039.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

Dated: April 24, 2002

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